ABSTRACT

A planar spin-on-glass layer over integrated circuits at the corners of chip areas is achieved. This allows more reliable integrated circuits to be made, and is useful for liquid crystal displays by eliminating optical distortion at the corners of the die areas. When a conducting layer is patterned to form portions of the integrated circuits over the chip areas, the layer is concurrently patterned to form a fill layer in the kerf areas. The spacings of the metal fill in the kerf areas are sufficiently narrow to provide a uniform coating of SOG over the corners of the die areas without buildup of the SOG. An oxide cap layer and a uniform SOG layer are deposited. The fill layer prevents dishing of the SOG layer when the SOG is polished back. The structure can be repeated for additional levels of electrical interconnections as required to complete the integrated circuits.